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EXAMINER	
ENG, MARSHALL S	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,125	ROONEY ET AL.	
	Examiner	Art Unit	
	Marshall S Eng	2133	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1.1 The drawings are objected to because Figure 13 contains two reference numbers 1303. From the specifications, it appears that the first reference 1303 that is directed to "determine a plurality of tests for a portion of an address space" should in fact be reference 1301.

1.2 The drawings are objected to because figures 3a-3c contain labels (i.e. X0, X1, X8, etc) that are illegible. Further, the figures (3a-3c) are too small to see/determine the features in each. Having each of the figures on its own diagram sheet so that the figures would be larger in size and therefore more readable/understandable is suggested.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2.1 The disclosure is objected to because of the following informalities:

- The word "of" should be inserted between the words "repetition" and "the" on line 11 page 10.
- The word "find" in the phrase "find numeral" on line 23 page 10 and subsequent occurrences is unclear. It appears that the word "find" is unnecessary.
- The word "and" in the phrase "and AND" on line 4 page 11 should be "an."

- The description of the superimposed combination 1, 3, 5, and 7 yielding a pass according to the Boolean AND operation on lines 1-8 of page 11 is unclear. It is further unclear how a pass is achieved as a result of the AND-ing of 3 passes and a fail.
- The number/variable(?) 10 on line 31 page 11 should apparently be "X10."
- The phrase "212" on line 18 page 15 should be "2^12."
- In lines 21-23, Figure 10 is described as being a circuit realization while, on line 7-8 of page 7 it is described as a flow diagram.

2.2 The disclosure is objected to because of the following informalities: the description of holding an address at a potential is not sufficiently described or explained in the abstract, the specifications (i.e. lines 20-24 page 3), or the claims. For the purposes of examination, however, it is being interpreted as holding an address at a specific value(i.e. 0 or 1) for the purposes of testing that address.

2.3 The disclosure is objected to because of the following informalities: the description of the test pattern on line 5 page 4 and line 11 page 5 appear to contradict themselves with the description of test patterns on line 9-10 page 4 and line 15-16 page 5. In the first description, the test pattern is said to "include a single address" while in the second description it is said that the test pattern "is a combination of at least one address." It is unclear whether the test pattern is meant to have a single address or at least one address.

2.4 The use of the trademark "Advantest" in line 8 of page 16 has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Appropriate corrections are required.

Claim Objections

3.1 Claims 1 and 10 are objected to because of the following informalities: the phrase "y addresses" in line 5 of claim 1 and line 3 of page 23 of claim 10 should be changed to "y address."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.2 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.3 Claim(s) 1-9 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. U.S. Patent No. 5,961,653 (hereinafter Kalter) in view of Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra).

AS per claim 1,

Kalter substantially teaches of using test patterns (that contain address sequencing (i.e. which addresses to test in order) to test portions of the address space, see column 1 lines 45-50. Kalter further of repeating the test patterns a plurality of times, see column 1 lines 47-50 where Kalter teaches of the test pattern continuously changing as the process matures. Since the process changes as it matures, the examiner is interpreting that the process is repeated plural times in order to mature and therefore go through changes.

Kalter does not explicitly teach of including at least an x and a y address, or of testing every combination by holding each address at a first potential and a second potential, or of determining and combining pass/fail information into a fail string. Nonetheless, Kalter does teach of using test patterns to test memories using data patterns, address sequencing and timing sequences, see column 1 lines 45-50.

Schanstra, in an analogous art, teaches of storing memory in a two-dimensional (i.e. x and y dimensions) array of memory cells, see section 2, column 2 on page 872.

Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads. Schanstra further teaches of using the pass/fail results of the read operations (tests), see section 2.1 column 1 on page 873. Further, Schanstra teaches that the bitmap is dependant upon the memory test algorithm used. It is clear that if only a certain section memory is to be tested (i.e. the test pattern address sequence) then the resulting bitmap will contain pass/fail information of the cells tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory testing of Kalter to include the teachings of Schanstra so as to enhance the memory testing capability of Kalter. This modification would have been obvious because of one ordinary skill in the art would have been motivated by the fact that the cited teachings of Schanstra are described as "the principles of memory testing and bit mapping," see column 1, last paragraph of section 1 on page 872 and as a result would have been both an easy and obvious step to include and implement.

As per claim 2,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the portion of address space to be tested to correspond to a number of addresses comprising the test pattern. Clearly, if the test pattern contains addresses to be tested, one of ordinary skill in the art would want those

addresses to correspond to the section/portion/area of memory that is being tested. If they did not, then the addresses to be tested would not correspond to the portion of memory, and no address (in the current portion/section) would be tested.

As per claim 3,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include a single address. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 4,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to hold the test pattern at a first potential and yield a pass/fail as well as to hold the test pattern at a second potential to yield a pass/fail. One of ordinary skill in the art would want to hold the test pattern at a first potential (i.e. 0) or a second potential (i.e. 1) so as to be able to test for, for example, stuck at high(1)/low(0) faults. Further, since Schanstra teaches of performing multiple reads (tests) per memory cell to obtain pass/fail information (section 2.1 column 1 on page 873), holding the cell at a certain potential long enough so as to obtain a pass/fail result would have been obvious as well. Since the purpose is to determine if a cell has passed or failed a memory test, then it would have been obvious to hold the cell at a value until a determination had been made.

As per claim 5,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include multiple addresses. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 6,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to determine the x and y addresses according to a targeted fail type. One of ordinary skill in the art would have chosen a fail type for testing and then chosen addresses appropriately. Further since only portions/sections/parts of the memory are being tested, then it would have been obvious to one of ordinary skill to select addresses of memory cells that fall within the current section to be part of the test pattern. Clearly, if addresses of cells not within the current section are chosen, then those cells would not be tested. Still further, the since the fail type is known, one of ordinary skill would know the characteristics of the fail type and clearly would have known which addresses to test to be able to detect the selected fault/fail type.

As per claim 7,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only

portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it.

As per claim 8,

Schanstra further teaches that a pass/fail cell is marked as a result of the cell passing or failing a test/read operation, see column 1 section 2.1 on page 873. While Schanstra does teach that a cell has failed if at least one test results in a fail, one of ordinary skill could easily lower the conditions for pass/fail so as to allow a pass result if at least one test results in pass or even if a certain percentage results in a pass.

As per claim 9,

Schanstra further teaches about the ability of BIST to be able to distinguish between fault types and locate the fault types, see column 2 section 3 on page 873. Since the pareto graph is essentially showing that faults types are not evenly distributed (i.e. only a few faults are responsible for the majority of the memory fails/defects) then it would have been an obvious step to one of ordinary skill in the art to take the fault distinguishing results and record them in the pareto chart/graph so as to be able to determine which faults cause the majority of the failures (i.e. the SC fail type in applicant's figure 1). One would be motivated to be able to determine which faults cause a majority of the failures so as to be able to take actions to prevent/remove those faults thereby causing less failures (and a getting higher yield).

4.4 Claim(s) 10-17 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. U.S. Patent No. 5,961,653 (hereinafter Kalter) in view of Schanstra et

al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra).

As per claim 10,

Kalter substantially teaches of using test patterns (that contain address sequencing (i.e. which addresses to test in order) to test portions of the address space, see column 1 lines 45-50. Kalter further of repeating the test patterns a plurality of times, see column 1 lines 47-50 where Kalter teaches of the test pattern continuously changing as the process matures. Since the process changes as it matures, the examiner is interpreting that the process is repeated plural times in order to mature and therefore go through changes.

Kalter does not explicitly teach of including at least an x and a y address, or of testing every combination by holding each address at a first potential and a second potential, or of determining and combining pass/fail information into a fail string. Nonetheless, Kalter does teach of using test patterns to test memories using data patterns, address sequencing and timing sequences, see column 1 lines 45-50.

Schanstra, in an analogous art, teaches of storing memory in a two-dimensional (i.e. x and y dimensions) array of memory cells, see section 2, column 2 on page 872. Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads. Schanstra further teaches of using the pass/fail results of the read

operations (tests), see section 2.1 column 1 on page 873. Further, Schanstra teaches that the bitmap is dependant upon the memory test algorithm used. It is clear that if only a certain section memory is to be tested (i.e. the test pattern address sequence) then the resulting bitmap will contain pass/fail information of the cells tested.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory testing of Kalter to include the teachings of Schanstra so as to enhance the memory testing capability of Kalter. This modification would have been obvious because of one ordinary skill in the art would have been motivated by the fact that the cited teachings of Schanstra are described as "the principles of memory testing and bit mapping," see column 1, last paragraph of section 1 on page 872 and as a result would have been both an easy and obvious step to include and implement.

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it. Further, Schanstra teaches of labeling a cell as a fail if any one of the multiple read/test operation results in a fail, see column 1 section 2.1 page 873. Therefore, the examiner sees the combination of the test results as an AND operation

where a pass could be regarded as '1' and a fail as a '0'. By combining using an AND operation, it ensures that either all of the tests are passes or else a fail is generated i.e. 1 AND 1 = 1/pass whereas 1 AND 0 = 0/fail.

Further, it would have been an obvious step to one of ordinary skill in the art to implement a method into programmed instructions that are executable by a storage device. Once the method is known/discovered, one of ordinary skill would easily be able to implement it in hardware using a plurality of devices as well as a set of programmable instructions readable by a program storage device/machine.

As per claim 11,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the portion of address space to be tested to correspond to a number of addresses comprising the test pattern. Clearly, if the test pattern contains addresses to be tested, one of ordinary skill in the art would want those addresses to correspond to the section/portion/area of memory that is being tested. If they did not, then the addresses to be tested would not correspond to the portion of memory, and no address (in the current portion/section) would be tested.

As per claim 12,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include a single address. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 13,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to hold the test pattern at a first potential and yield a pass/fail as well as to hold the test pattern at a second potential to yield a pass/fail. One of ordinary skill in the art would want to hold the test pattern at a first potential (i.e. 0) or a second potential (i.e. 1) so as to be able to test for, for example, stuck at high(1)/low(0) faults. Further, since Schanstra teaches of performing multiple reads (tests) per memory cell to obtain pass/fail information (section 2.1 column 1 on page 873), holding the cell at a certain potential long enough so as to obtain a pass/fail result would have been obvious as well. Since the purpose is to determine if a cell has passed or failed a memory test, then it would have been obvious to hold the cell at a value until a determination had been made.

As per claim 14,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to make the test pattern include multiple addresses. Test patterns contain address sequencing (i.e. which addresses to test). Therefore, it would have been obvious to one of ordinary skill in the art to have the test pattern include at least a single address to test.

As per claim 15,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to determine the x and y addresses according to a targeted fail type. One of ordinary skill in the art would have chosen a fail type for testing and then

chosen addresses appropriately. Further since only portions/sections/parts of the memory are being tested, then it would have been obvious to one of ordinary skill to select addresses of memory cells that fall within the current section to be part of the test pattern. Clearly, if addresses of cells not within the current section are chosen, then those cells would not be tested. Still further, the since the fail type is known, one of ordinary skill would know the characteristics of the fail type and clearly would have known which addresses to test to be able to detect the selected fault/fail type.

As per claim 16,

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo compressed bitmap comprising cells that are either of a passing or failing type. One of ordinary skill in the art would know that the cells are marked passing or failing in the bitmapping process of Schanstra, see claim 1 above and column 1 section 2.1 on page 873 of Schanstra. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it.

As per claim 17,

Schanstra further teaches that a pass/fail cell is marked as a result of the cell passing or failing a test/read operation, see column 1 section 2.1 on page 873. While Schanstra does teach that a cell has failed if at least one test results in a fail, one of ordinary skill could easily lower the conditions for pass/fail so as to allow a pass result if at least one test results in pass or even if a certain percentage results in a pass.

4.5 Claim(s) 18-19 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Schanstra et al. "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories" (hereinafter Schanstra).

As per claim 18,

Schanstra substantially teaches of marking cells as passing or failing during a bitmapping process, see column 1 section 2.1 on page 873. Further, since only portions of the memory is being tested, then the bitmap generated would be pseudo compressed in the sense that the entire bitmap is not being displayed, and only a small portion of it. Further, Schanstra teaches of labeling a cell as a fail if any one of the multiple read/test operation results in a fail, see column 1 section 2.1 page 873. Therefore, the examiner sees the combination of the test results as an AND operation where a pass could be regarded as '1' and a fail as a '0'. By combining using an AND operation, it ensures that either all of the tests are passes or else a fail is generated i.e. 1 AND 1 = 1/pass whereas 1 AND 0 = 0/fail.

While Schanstra does not explicitly teach of having the pass/fail results correspond to X and Y address pins, Schanstra does teaches of the memory being stored as a two-dimensional array of memory cells, see column 2 section 2 page 872. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the addresses of the pass/fail results (cells) correspond to X and Y address pins. One of ordinary skill in the art would know that memory (i.e. those in array form) are addressable through pins. Since the pass/fail results correspond to cells, then it would have been obvious to make the address of the cell

with pass or fail result be addressable by an X (x-axis direction) and Y (y-axis direction) pin.

As per claim 19,

Schanstra further teaches of performing more than one read operation per memory cell, see section 2.1 column 1 on page 873. The examiner is interpreting that performing multiple reads per memory cell that the same or different data (i.e. 0 or 1; therefore all combinations) is being written to and expected to be read out during each of the multiple reads.

Conclusion

5.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Augarten U.S. Patent No. 5,588,115

b. Heaslip et al. U.S. Patent No. 6,643,807

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marshall S Eng whose telephone number is (703) 305-4638. The examiner can normally be reached on M-Th, 9 am to 5:30 pm and F, 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mse

Albert DeCady
Primary Examiner